



## The challenges of the new global scenario



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### Goal

- The lecture is aimed at outlining where most of today designers' constraints come from.
- Thus it first presents the current trends in the microelectronic industries, with particular emphasis on System-on-a-Chip.
- It then outlines the various phases of a product life cycle, focusing on Concurrent Engineering approaches.

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### Homework

- Students are warmly invited to visit:
  - web pages related to microelectronic trends, such as:
    - The International Technology Roadmap for Semiconductors home page at <http://public.itrs.net>

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### Homework (cont'd)

- web pages related to on-going standardization activities on System-on-a-Chip, such as:
  - VSI Alliance home page at <http://www.vsi.org/>
  - IEEE P1500 Standard for Embedded Core Test (SECT) home page at <http://grouper.ieee.org/groups/1500/>

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### Further readings

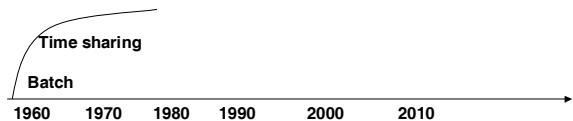
- No particular suggestion

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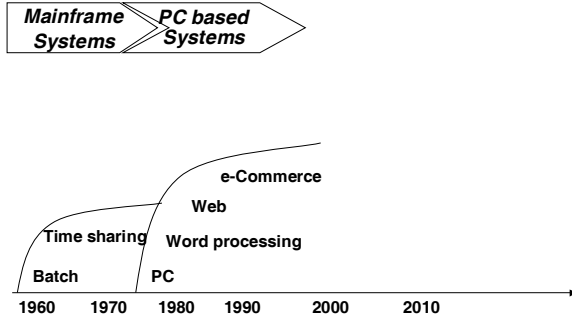
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### Waves of electronic computing

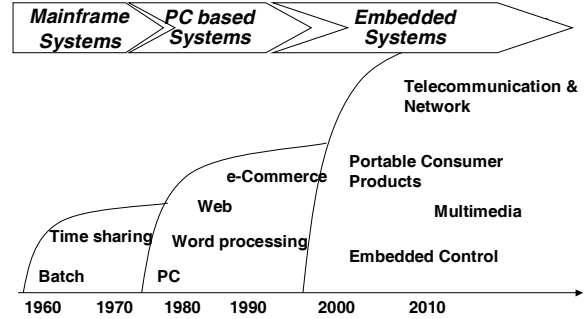
Mainframe Systems



**Waves of electronic computing**



**Waves of electronic computing**



**Two forces working in conjunction in electronics industry**



**Two forces working in conjunction in electronics industry**



**Consumerization of the microelectronic industry**

- High volumes



**Some facts ...**

- 50 millions of Pentium produced every year (1 Pentium every 0.6 s!!)
- 100 millions of PC and 3 millions of servers sell in '99
- ...





**Consumerization of the microelectronic industry**

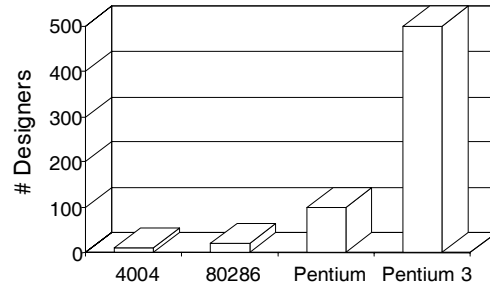
- High volumes
- High costs for design and production

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**High costs for design**

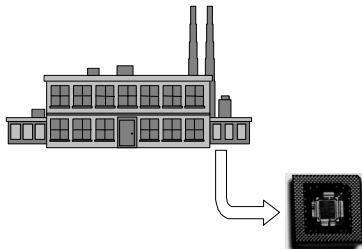


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**High costs for production**

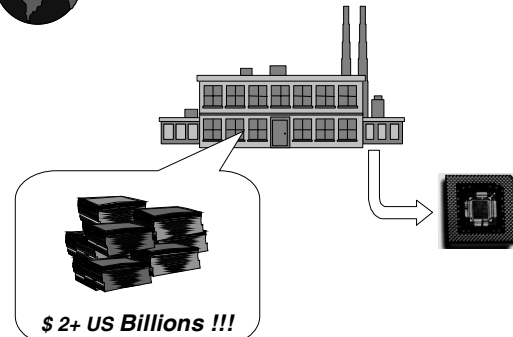


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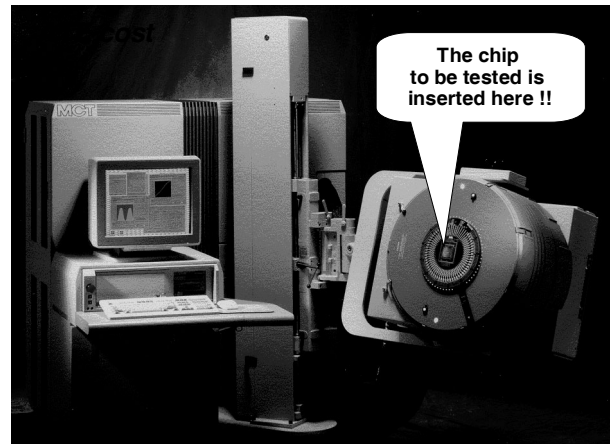
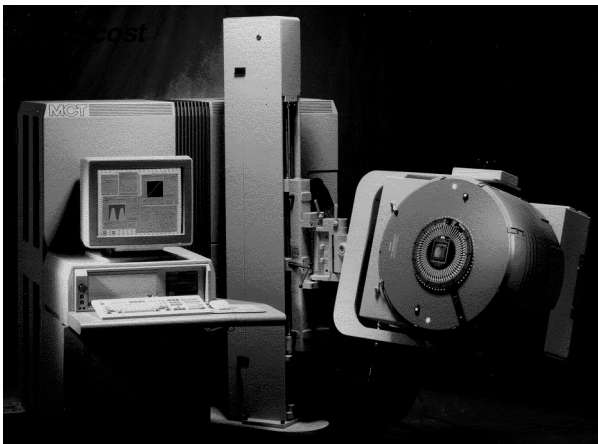


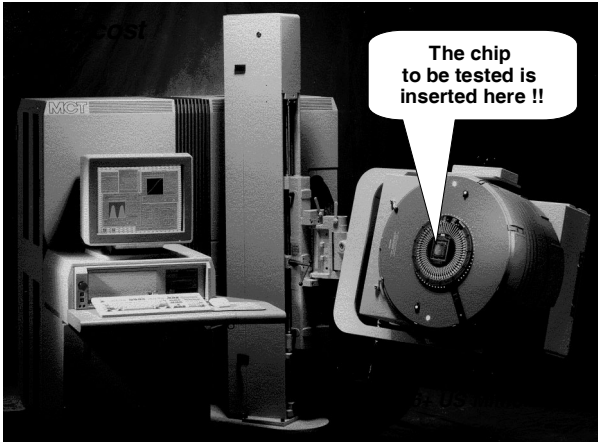
**High costs for production**



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**Some facts: Pentium Intel**



- For End-of-Production test, Intel uses 300 ATEs for VLSI:
  - if aligned, they formed a 2 Km queue
  - they have, globally, 60,000 pin drivers
  - they consume, globally, 7.5 MW.

[K. Thompson, Vice president Intel, ITC'95]

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**Consumerization of the microelectronic industry**

- High volumes
- High costs for design and production
- Lower prices of the final products

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**Some facts ...**

Since 1Q'97, the price of PCs decreases of 6% every quarter.

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**Consumerization of the microelectronic industry**

- High volumes
- High costs for design and production
- Low prices of the final products
- High dependability (reliability & availability)

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**Two forces working in conjunction in electronics industry**





### Moore's law

Processor transistor counts doubles every two years



- a new technology every 9 months !!
- System-on-a-chip (SoC)

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### Pentium 4

- 1.5 GHz → 2 GHz in 3Q01
- 0.18 μ → 0.13 μ in 4Q01
- 42 M transistor

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### Intel Press release

"Researchers at Intel Corp. have built what they claim is the smallest and fastest CMOS transistor, measuring 30nm in size and three atom thick. The gate oxides used to build these transistors are three atomic layers thick.

Intel believes this new development will allow the company within the next five to 10 years to build microprocessors containing more than 400 million transistors, running at 10GHz and operating at less than 1V.

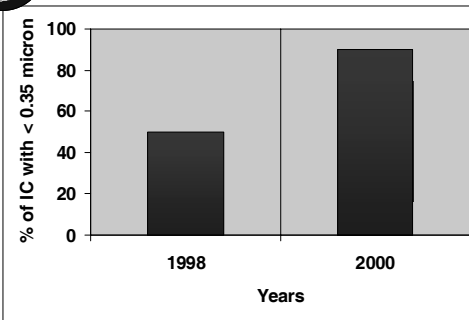
To rationalize this scale, Intel said more than 100,000 of these gates would need to be stacked to achieve the thickness of a sheet of paper and that they could compute 2 million calculations in the time it takes a bullet to travel one inch."

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### Very deep sub-micron ICs

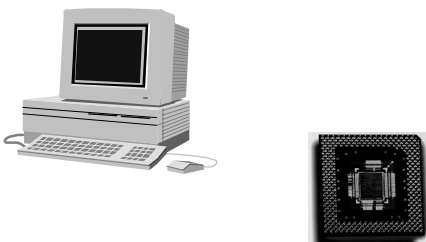


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### System - chip

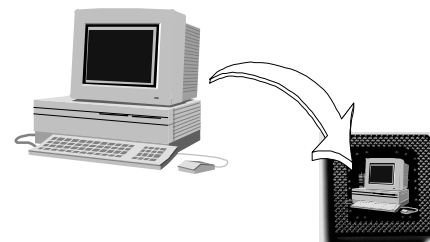


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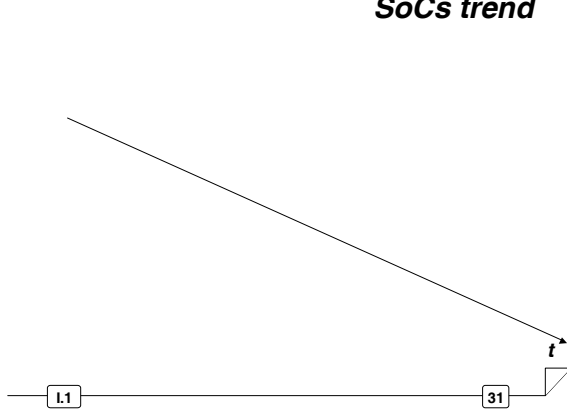
### System-on-chip



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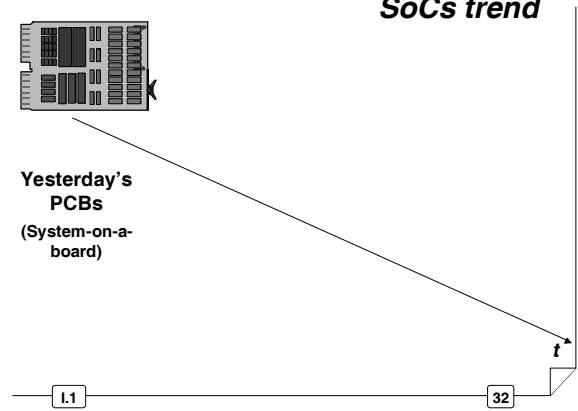
**SoCs trend**



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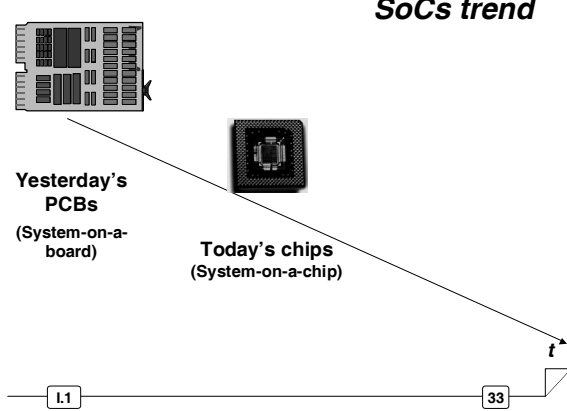
**SoCs trend**



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**SoCs trend**



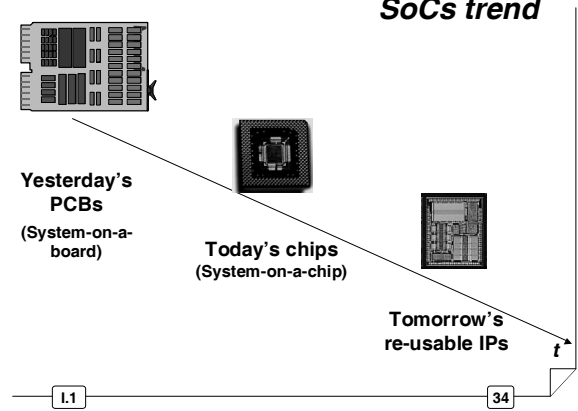
Yesterday's  
PCBs  
(System-on-a-board)

Today's chips  
(System-on-a-chip)

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**SoCs trend**



Yesterday's  
PCBs  
(System-on-a-board)

Today's chips  
(System-on-a-chip)

Tomorrow's  
re-usable IPs

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**What are embedded cores**

Pre-designed, pre-verified functional blocks, also termed *IP* (Intellectual Property), or *macro*.

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**Characteristics of Core-based SoCs**

- Reusable cores replacing existing COTS ICs
- Core representation at different hardware description level (soft, firm, hard)
- Embedded cores available from diverse sources
- Design efficiency achieved by ease of *plug & play* (a lot of standardization activities are currently going on).

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**SoC market growth**

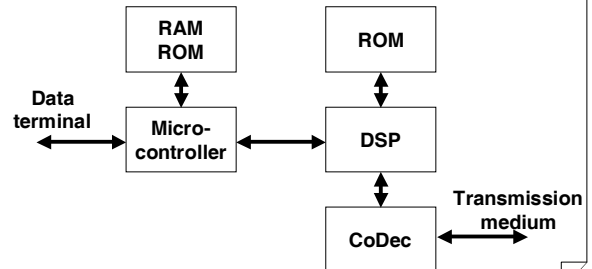
1998	9.0
1999	11.0
2000	14.5
2001	19.0
2002	24.0
2003	32.0

Worldwide revenue (B of \$)  
[Dataquest]

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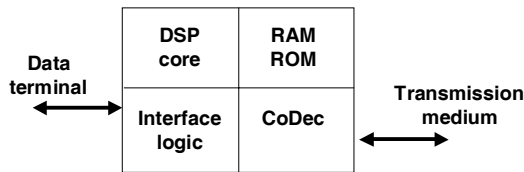
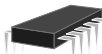
**Example:  
A mixed signal modem  
(board implementation)**



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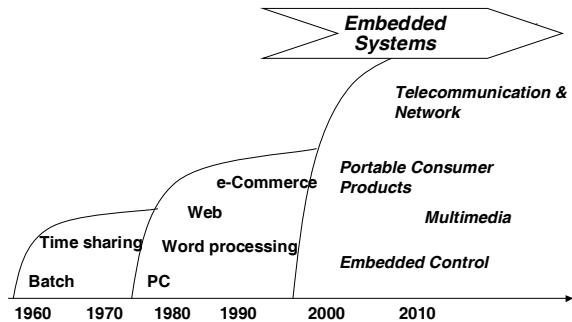
**Example:  
A mixed signal model  
(SoC implementation)**



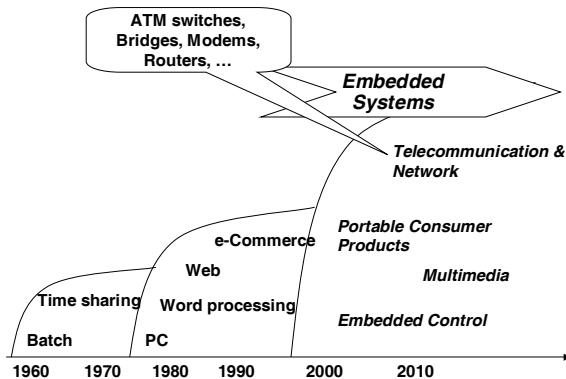
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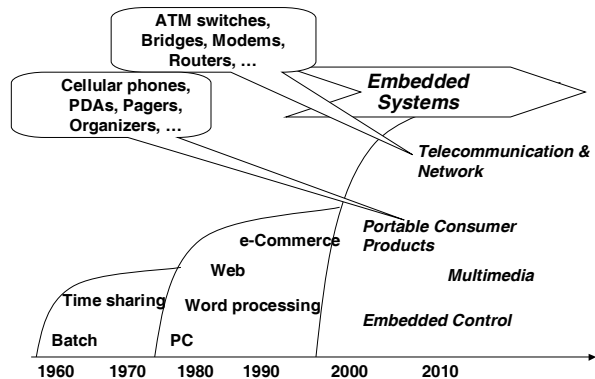
**Target Applications**

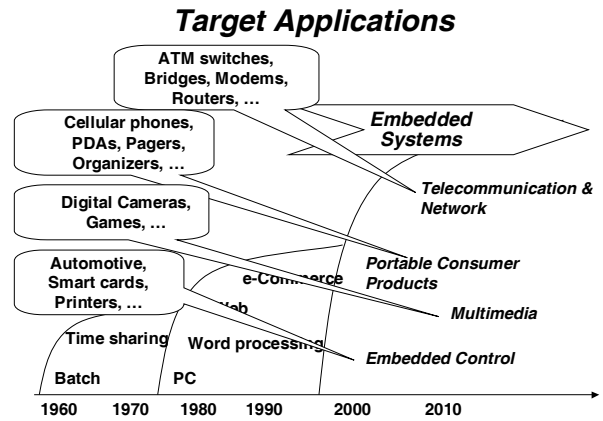
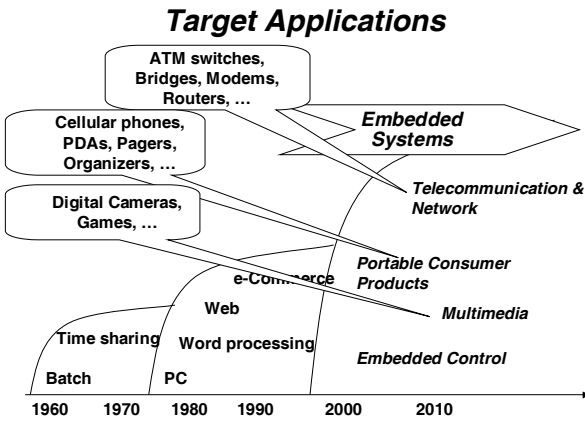


**Target Applications**

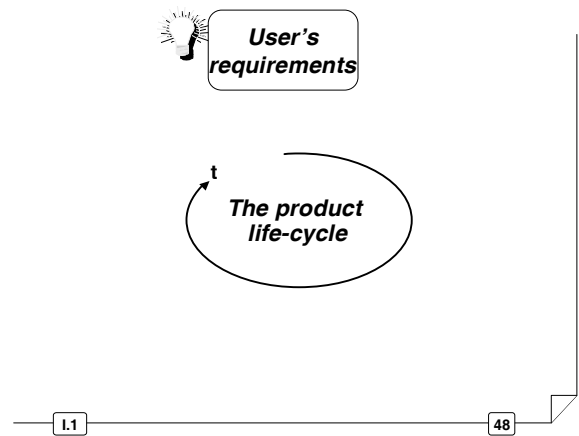
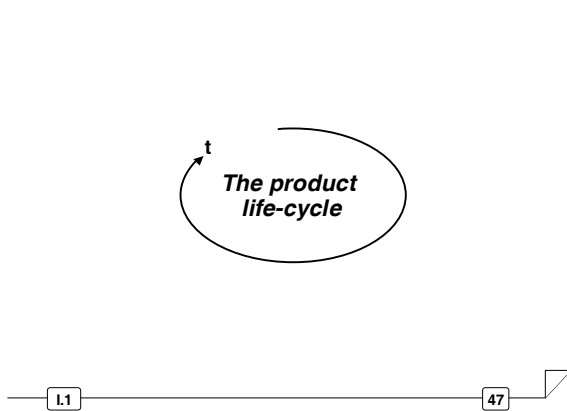


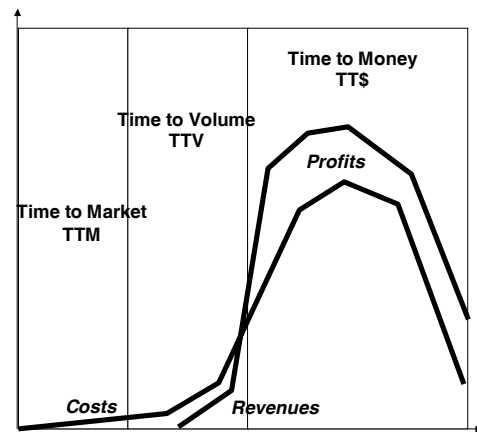
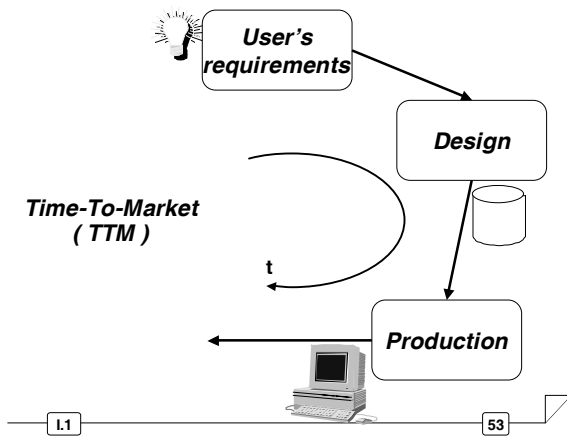
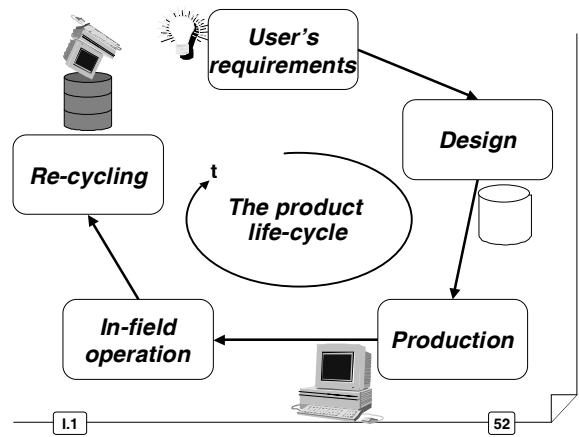
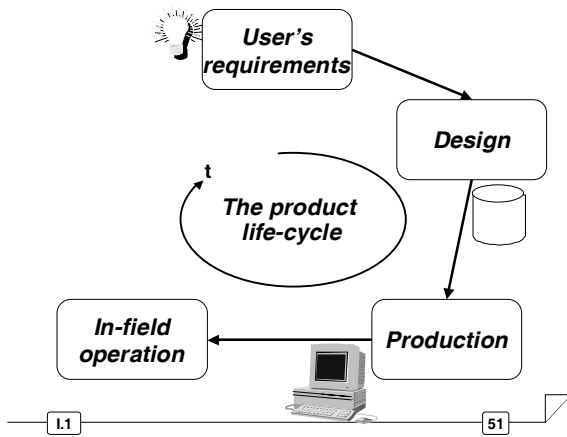
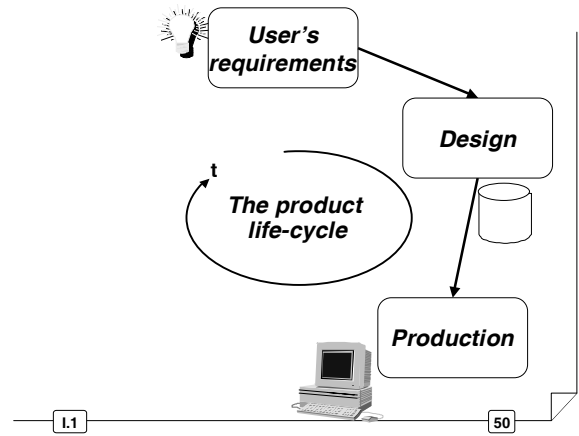
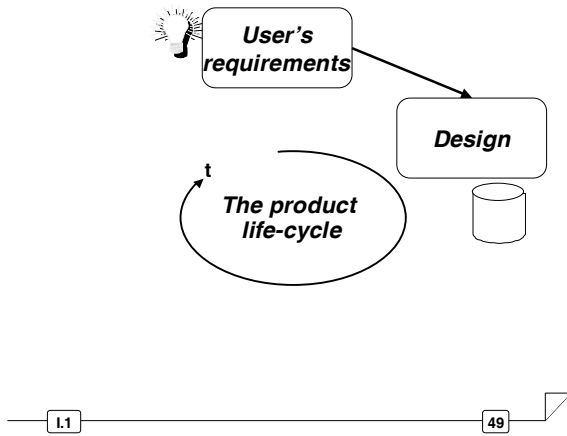
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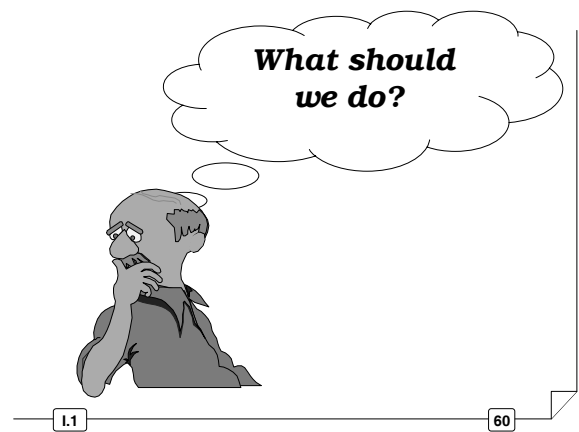
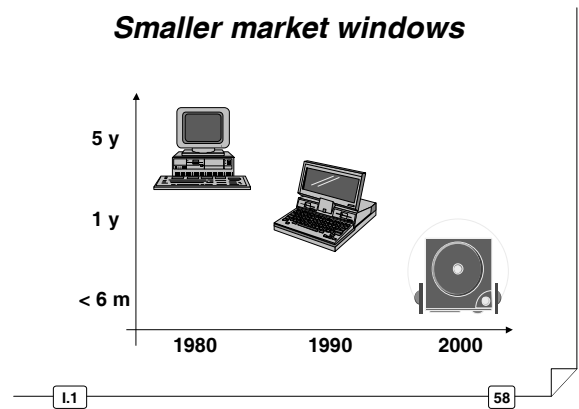
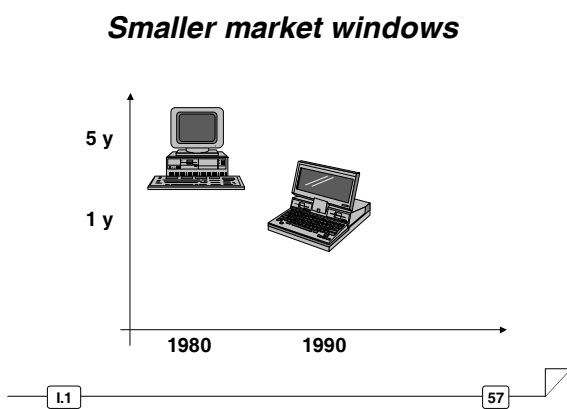
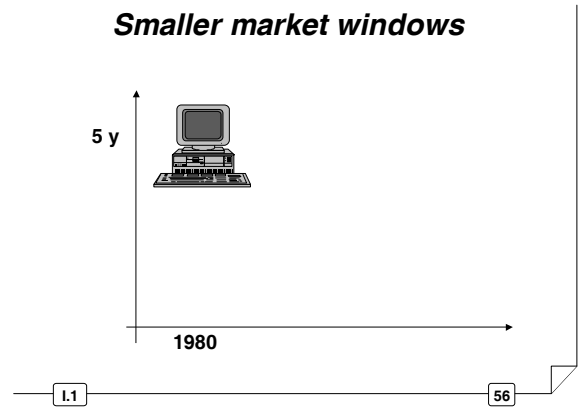
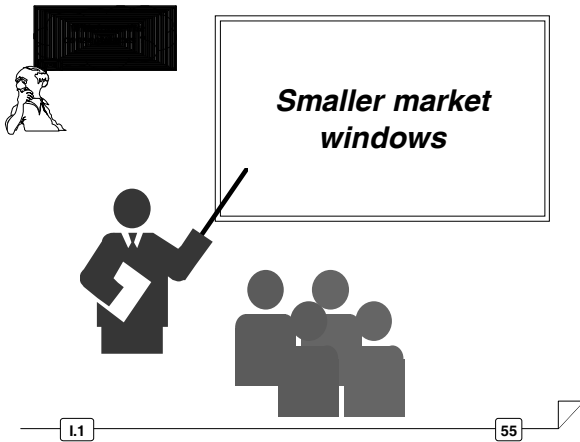




- Just few reminds ...**
- Product life cycle
  - Time to Market
  - Time to Volume
  - Time to Money
  - Market Window
- I.1 46







What should we do?

**To survive, you must be able to meet the trends.**

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What should we do?

**The real challenge:  
To meet user quality requirements for your new products**

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**Quality**

*The set of properties and characteristics of a product (a service) capable of guaranteeing customer's satisfaction.*

ISO 8402

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**The quality of any product or service is what the customer says it is.**

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What should we do?

**Reduce your Time-To-Market**

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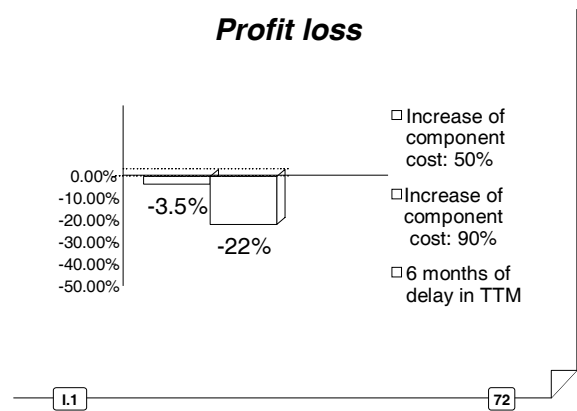
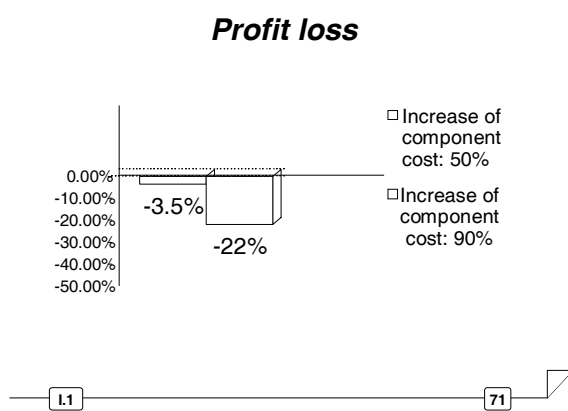
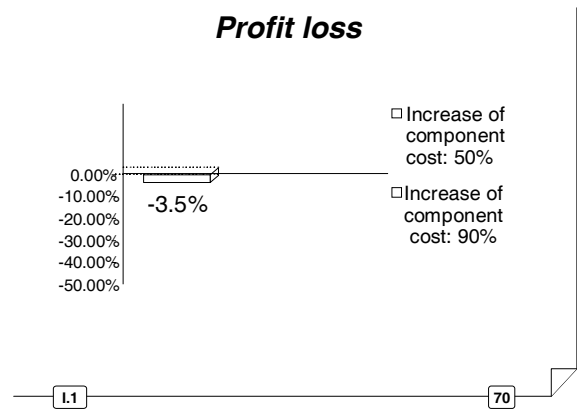
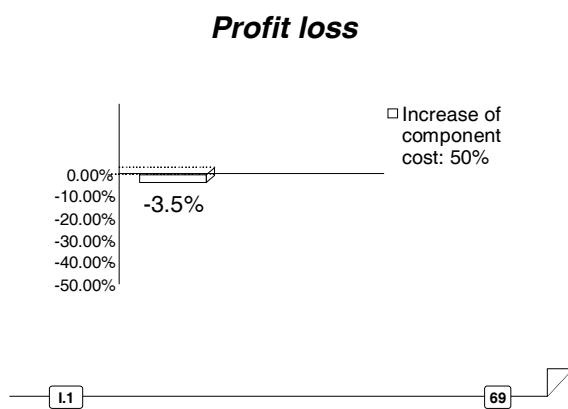
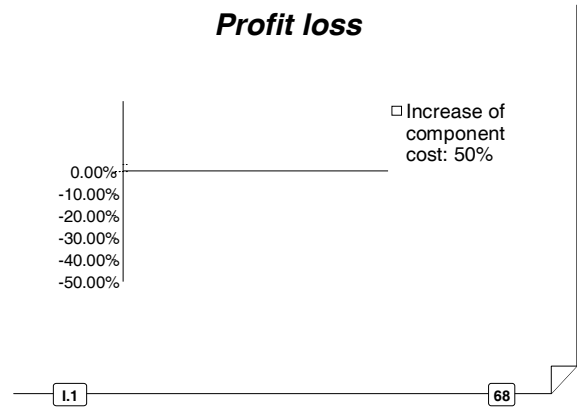
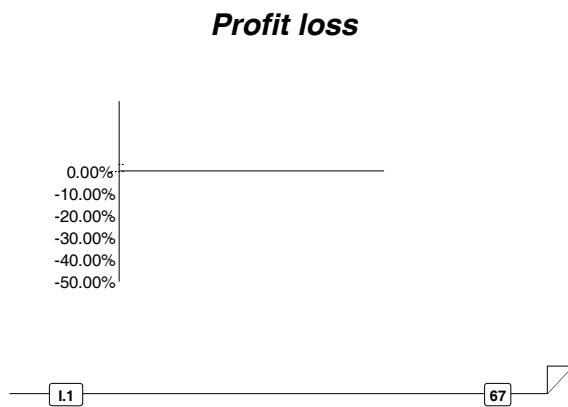
**The impact of delay on profits**

Let's consider a product characterized by:

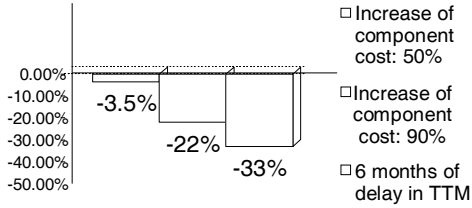
- market grow rate : 20%
- annual price reduction rate : 12%
- product life-cycle: 5 y

[McKinsey & Co]

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**Profit loss**



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**How can we reduce our TTM ?**



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*How can we reduce our TTM ?*



**Set up Distributed Cooperative Working Environments to support Concurrent & Distributed Engineering**



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*Concurrent Engineering is a systematic approach to the integrated, concurrent design of products and their related processes, including manufacture and support.*

[Institute for Defense Analyses, USA]

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*Concurrent Engineering is intended to cause the developers, from the outset, to consider all the elements of the product life cycle from conception through disposal, including quality, cost, schedule, and user requirements.*

[Institute for Defense Analyses, USA]

[IEEE Spectrum, July 1991]

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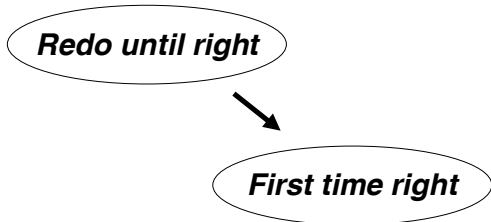
**Concurrent Engineering**

**Redo until right**

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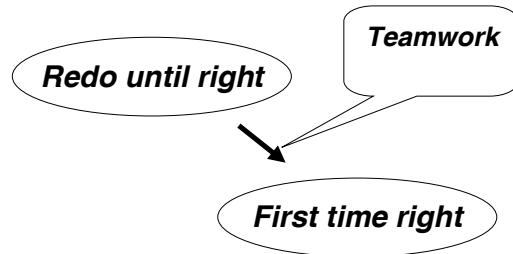
Concurrent Engineering



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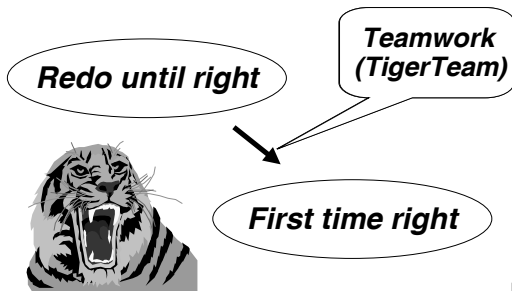
Concurrent Engineering



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Concurrent Engineering



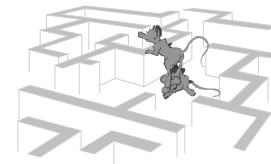
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TigerTeam

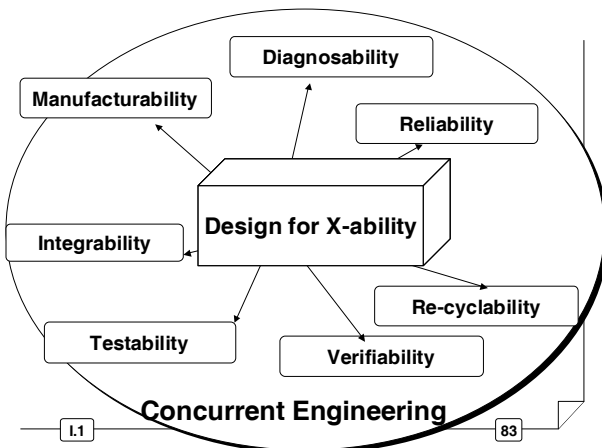


People from many departments collaborate over the life of a product to ensure that it reflects customers' needs and desires.



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Concurrent Engineering

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Some examples ...

- **Boeing Corporation Airplane Group:**  
**Boeing 777** (440 passengers) developed in 1.5 years less than 767:
  - 2200 terminals
  - 8 mainframes IBM 3090-600J
  - connected Seattle, Renton, Everett (DC), Wichita (KA), Philadelphia (PA) & partners like Mitsubishi, Kawasaki, Fuji

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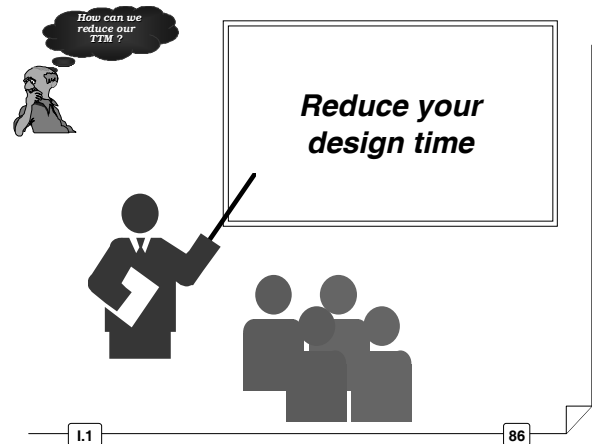
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### Some examples ...

- **FIAT:**  
300 people to design and set up the PUNTO production line
- **IBM, Apple, Motorola:**  
PowerPC 601: 12 months from agreement signature to the first chip.

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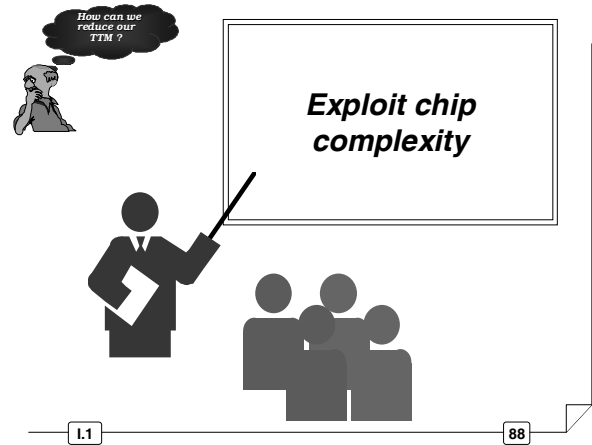
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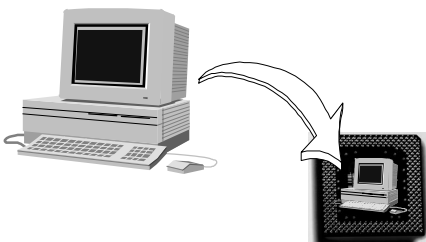


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### System-on-chip



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