



An Introduction to Automated Synthesis



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Goal

- This lecture presents a brief introduction to Automated Synthesis.

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Prerequisites

- Module 4

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Homework

- No particular homework is foreseen

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Further readings

- No particular homework is foreseen

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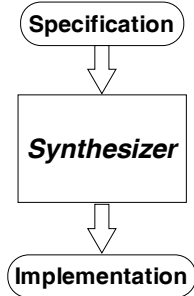
"Civilization advances by extending the number of important operations we can perform without thinking of them"

[A. Withehead]

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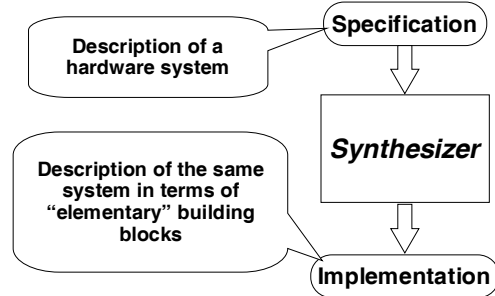
Automated Synthesis



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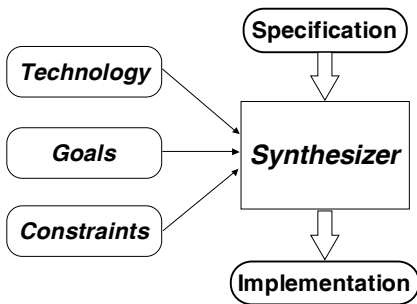
Automated Synthesis



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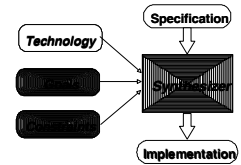
Synthesis inputs



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Technology



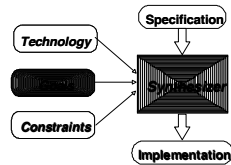
Characteristics of the physical implementation:

- available elementary blocks
- characteristics of each block (function, area, delay, power consumption, fanin, fanout, ...)
- ...

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Constraints



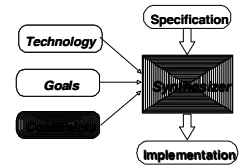
Outside constraints imposed by the environment:

- arrival times for input values
- max delay on outputs
- ...

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Goals



Drive the synthesis flow to optimize:

- speed
- area
- power consumption
- testability
- ...

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**Goal #1:
coherency with specification**

Real goal:

“what you *specify* is what you *synthesize*”

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**Goal #1:
coherency with specification**

Real goal:

“what you *specify* is what you *synthesize*”

The meaning (semantics) of the specification is defined by its simulated behavior:

“what you *simulate* is what you *synthesize*”.

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“What you *simulate* is what you *synthesize*” : problems

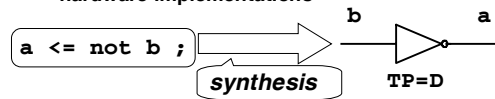
- VHDL semantics is often ambiguous
- VHDL may exhibit behaviors not matched by hardware implementations

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“What you *simulate* is what you *synthesize*” : problems

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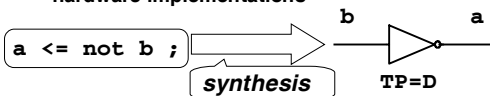


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“What you *simulate* is what you *synthesize*” : problems

- VHDL semantics is often ambiguous
- VHDL may exhibit behaviors not matched by hardware implementations



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**Goal #2:
constraints satisfaction**

The synthesis tool must:

- accurately evaluate area occupation
- accurately evaluate propagation delays
- identify critical paths

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**Goal #3:
realization in the technology**

The same logic function must be realized differently, depending on the available blocks in the library.

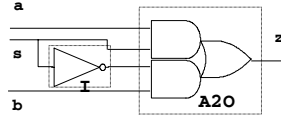
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**Goal #3:
realization in the technology**

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$$z \leq (a \text{ and } s) \text{ or } (b \text{ and not } s);$$



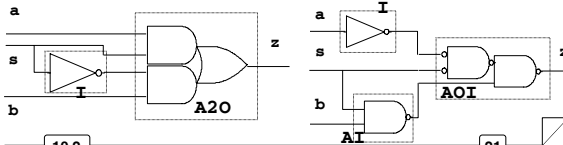
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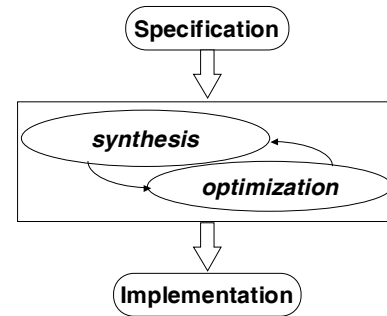
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Typical architecture



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