

Dielectric Materials in Organic Thin Film Transistors

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This work focuses on dielectric materials in organic thin film transistors. Silicon oxides whose surfaces are modified with hexamethyldisilazane (HMDS) and octyltriethoxyl Silane (OTS) are investigated. Organic semiconducting materials are used in the transistors made within the scope of this work. Although the devices made using our procedures did not exhibit satisfactory performance, we explored and understood some chemical and engineering aspects of the relevant dielectric/semiconductor interfaces in organic thin film transistors. Understanding these systems would help with improvements of the electrical properties and performance of such systems when plastic substrates are used at the next stage of the project.

Introduction

There has been an increasing interest into the use of organic materials as alternatives to traditionally used inorganic metals like silicon. These organics are of interest because they can be processed at low temperatures over large areas on materials such as plastic or paper.¹ Such advantages make the use of organics less expensive. However due to low mobility of organic semiconductors, Organic Thin-Film Transistors (OTFT) are not as effective as single-crystalline inorganic semiconductors.² Silicon (*Si*) and Germanium (*Ge*), for example, have carrier mobilities three orders of magnitude higher than those of the organics.² It has also been shown that the crystal structure of the pentacene semiconductor affects the mobility.¹ These materials have conducting or semiconducting properties due to π -orbital overlap of neighboring molecules.² This π -orbital overlap is enhanced by the self-assembling or ordering of these organics.² Being able to get good crystal structure would be important in order to get optimal electrical properties of potential candidate materials.

We are still working on getting good crystal structure for the semiconductor as well as being able to apply the dielectric material on the surface. The dielectric material would consist of polymers or layers of organic materials. *Si* substrate is initially being used because it has been well studied. As we learn more about functional group interactions and the chemistry of the *Si/SiO₂* surface, we would be able to use this knowledge in systems that would include plastic substrates.

Methods

Deposition methods that were used included spin-coating, pad printing, and screen printing. These methods are used because they can be done at low temperatures, they can be used on plastic substrates, and they can result in thin layers of the material of interest.

The crystalline solution processable pentacene organic semiconductor material was obtained from a Motorola vendor. These organic semiconductors have high mobility and are suitable in Organic Thin Film Transistors (OTFT). Heavily doped silicon is the substrate and gate material; silicon dioxide is grown on top of the silicon wafer as a dielectric and then it is modified by Hexamethyldisilazane (HMDS) and Octyltriethoxyl-Silane (OTS). Source and drain are deposited on the dielectric by pad printing or screen printing method. Both printing methods are contact printing. For pad printing, the printed image is etched on a metal plate (cliché), the cliché is inked with pad printable ink, and the ink pattern on the cliché is picked up by a rubber stamp which transfers the pattern on to a substrate. For screen printing, the image is predefined on a silk screen; the ink is transferred on the substrate by squeegee the ink through the silk screen. The methods of deposition used for the organic materials are solution-based.

Characterization techniques that were used are Fourier Transform Infrared (FTIR) Spectroscopy, Keithley Systems, and WYKO RST PLUS (Roughness/Step Tester) System. FTIR spectroscopy is used to probe the bonding before and after surface modification. Keithley Systems is used to measure the electrical properties, that is,

the current-voltage (I-V) curve, capacitance, on/off ratio, and threshold voltage of the devices made. WYKO RST PLUS is used to get surface roughness and related imaging. These properties, in addition to the thickness of the material(s) and channel size, are used to calculate the mobility and dielectric constant.

Experimental

Reagents

The chemicals we used are HMDS, Hydrogen peroxide (H_2O_2), sulfuric acid (H_2SO_4), and OTS by Aldrich-Sigma. The structures of HMDS and OTS are shown below (Figure 1). All materials were used as supplied.

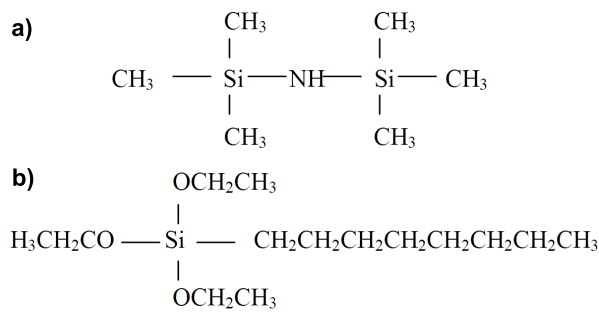


FIG. 1: Chemical Structure of a) HMDS and b) OTS.

Procedure

The Silicon wafer was cut into a $1.5 \text{ cm} \times 1.5 \text{ cm}$ square then cleaned using piranha solution consisting of H_2O_2 and H_2SO_4 in 1:3 ratio, rinsed with distilled water, and dried with nitrogen gas before being placed in the oven. The clean silicon wafers are then put in an oven at 1000°C , 1 atm , $3.5 \frac{\text{l}}{\text{min}}$ flow of oxygen for a certain amount of time to get desired thickness of SiO_2 . The SiO_2 thicknesses obtained are about 60, 100, and 350 nm after processing for 30 min, 1 hr, and 5 hr, respectively. Next, the wafer with SiO_2 on its surface is treated again with the piranha solution at 80°C for 20 min, rinsed with DI water, and dried in N_2 again. This step is done in order to make the $-OH$ group on the Si surface. $Si-OH$ can then react with both HMDS and OTS.

HMDS Treatment

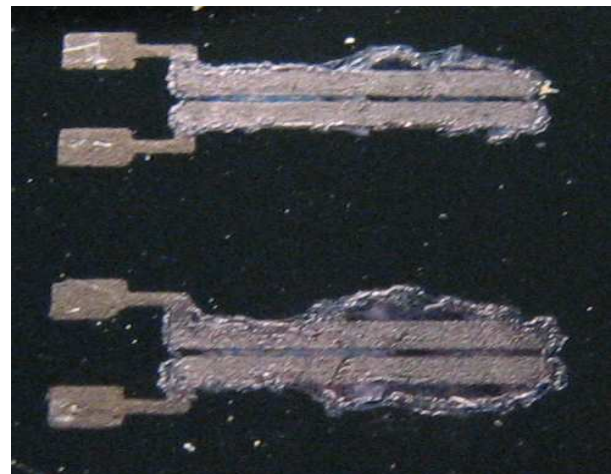
After SiO_2 has been grown and reacted with the piranha solution, a monolayer of $-OH$ is in the form of $Si-OH$. The $Si-OH$ wafer is placed in HMDS at 120°C for 1 hr, washed with acetone to remove excess HMDS, rinsed with DI water, and dried again with blowing N_2 gas.

After treating the wafer, we spin coat the semiconductor material, bis(triisopropylsilyl)ethynyl)pentacene (TIPS-pentacene), dissolved in toluene to get 1 % solution on the three different surfaces: silicon oxide, $Si-OH$, and HMDS treated surfaces. We then pad print source and drain from carbon suspension in organic solvent, and consequently cure it in oven at 110°C for 15 min. The resulting structures are characterized using FTIR spectroscopy and ellipsometric analysis (to measure the thickness).

OTS Treatment

The $Si-OH$ wafer is placed in a solution of OTS before it is placed in a 70°C oven for 30 min. The wafer is then moved to a 120°C oven for 15 min in order to allow the evaporation of OTS. Excess OTS is rinsed off using acetone.

Following the surface modification, we make the device. Unlike the procedure used with HMDS, the source and drain is pad printed first and cured in an oven at 110°C for 15 min. The pentacene-based semiconductor is deposited between the source and drain channel using a pipette and is treated in an 110°C oven for about 30 sec. A picture of the resulting transistor obtained with a digital camera is shown in Figure 2.



Channel Length: 5000 μm

Channel Width: 100 μm

Source and Drain Width: 500 μm

FIG. 2: Picture of a transistor: source and drain on octyltriethoxysilane (OTS) modified surface and organic semiconductor deposited in the channel between source and drain.

Results and Discussion

The devices were initially made with 100 nm-thick SiO_2 grown on the heavily-doped Si substrate and HMDS modification did not result in good performance. Thus, we used 60 nm-thick SiO_2 in order to study whether our finding was the result of having grown SiO_2 that is too thick. However after depositing the semiconductor on the surface of the 60 nm-thick oxide, measured currents on the surface showed that the device was already shunt. We also used a 350 nm-thick SiO_2 , and the device was not shunt after the TIPS- pentacene. This suggested that 100 nm-thick SiO_2 was most likely too thin for this device system.

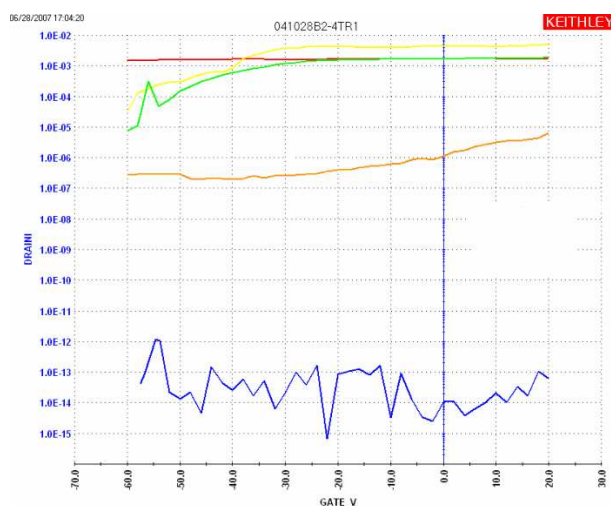


FIG. 3: Gate voltage versus drain current for a transistor made out of 100 nm-thick SiO_2 . Red and Orange lines represent the devices made on SiO_2 surface, yellow and green lines are for devices on $\text{Si}-\text{OH}$ surface, and blue line is for devices on HMDS treated surface.

Figure 3 shows the results obtained after making the device on the 100 nm-thick silicon oxide. None of the devices turned on or off. The red, yellow and green lines in Figure 3 show that the source and drain touch each other, since the drain current remains the same when the gate voltage changes. This could be caused by the printing method used. Although the orange and blue lines show that source and drain are not shunt, there is still no switching on and off. This could be due to small amount of crystals of semiconductors or disorder crystals in the channel. The low drain current for the device on the HMDS treated surface, which is presented with the blue line, indicates there is no leakage through the dielectric; however, there is leakage in the devices based on non-treated SiO_2 . Figure 4, for the OTS-treated surface does not show a switching behavior; instead, the sharp turn at minimum shows that the source and drain are shunt, since there is a sharp turn around the bias voltage, -40 V.

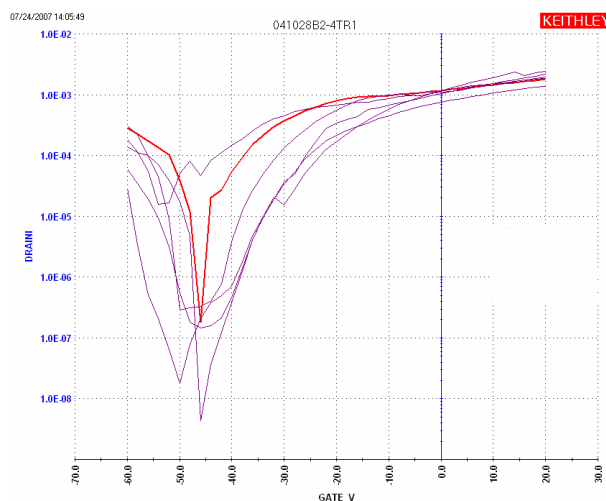


FIG. 4: Graph showing drain current versus gate voltage of transistors made on OTS treated SiO_2 surface that is 350 nm-thick.

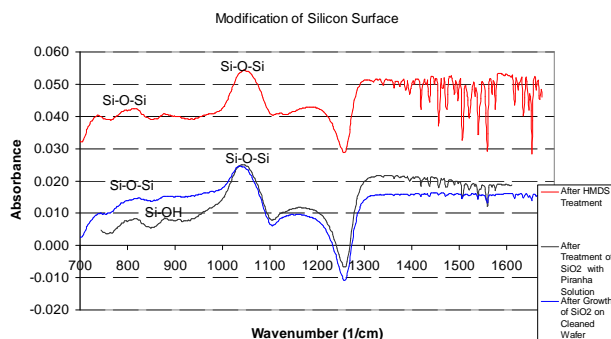


FIG. 5: FTIR spectra of a 100 nm-thick SiO_2 surface after each step leading to HMDS surface modification.

FTIR absorption spectroscopy was also used to track molecular bonding on the surface of the wafer before and after the modifications used. Figure 6 shows the results obtained from the surface modification steps of the 100 nm-thick SiO_2 . There is a small peak showing the $\text{Si}-\text{OH}$ bond on the piranha solution-treated surface, but $-\text{OH}$ groups on the surface make a monolayer that it is too thin to be detected by FTIR; therefore, they also could come from moisture.

From the next processing step, which is the reaction of the hydrated surface with HMDS, the attachment of HMDS onto the surface suggests that $-\text{OH}$ groups had been attached since HMDS only reacts with $-\text{OH}$ on the surface. When FTIR spectroscopy was used to analyze the surfaces of the wafer leading up to the OTS treatment, there was no significant change. The absence of the $-\text{OH}$ peak may be due to what has already been discussed above. Also, the absence of any $-\text{CH}_3$ peaks suggests that the binding of OTS is due to a very thin

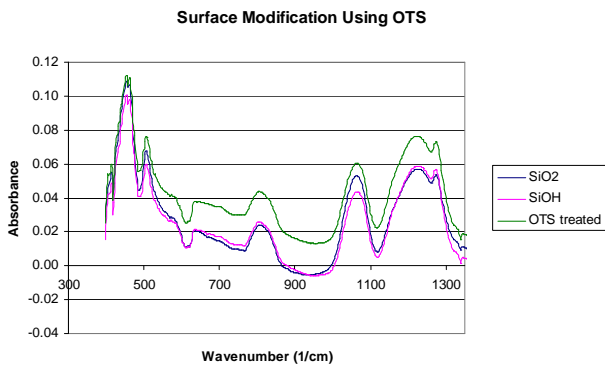


FIG. 6: FTIR spectra of the surface modification steps using OTS. Blue: After growing SiO_2 ; Pink: after treatment with piranha solution to get $-OH$ on the surface; Green: after OTS treatment.

layer of OTS. Figure 6 shows the FTIR spectra of the SiO_2 , $Si-OH$, and OTS-treated surfaces. Using contact angle measurements, OTS and HMDS was apparently bonded to the surface as evidenced by the hydrophobicity of the resulting surfaces. The specific contact angle results obtained with a micro-droplet of water on the related surfaces are summarized in Table I.

Surface	Approx. Contact Angle
SiO_2	30
$Si-OH$	30
HMDS treated	70
OTS treated	90

TABLE I: Contact angle measurements using a micro-drop of H_2O on the surfaces of interest.

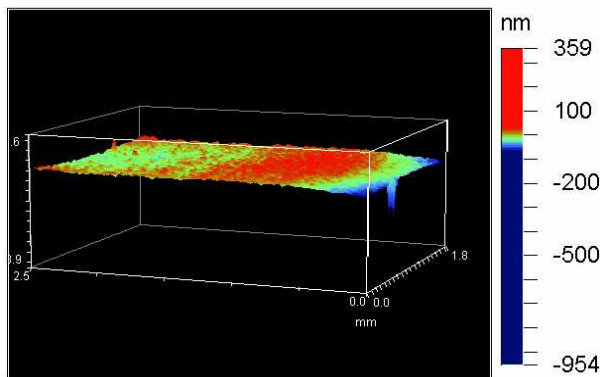


FIG. 7: Image of a 350 nm-thick SiO_2 surface showing the roughness of the surface.

We were also able to get the surface roughness using WYKO RST PLUS (Roughness/Step Tester) System. Figure 7 and 8 show the SiO_2 and OTS treated surfaces. Table II includes the average roughness data that

was collected on the surfaces of interest. The rougher the surface is before the deposition of the semiconductor, the less uniform the crystal structure of the semiconductor deposited. As indicated earlier, the crystal structure of the semiconductor then affects the electrical properties of the transistor.

Surface (> than 100 nm thick Si)	Avg. Roughness (nm)
Si / Substrate	17
SiO_2	12
OTS treated	17

TABLE II: Average roughness of the surfaces investigated.

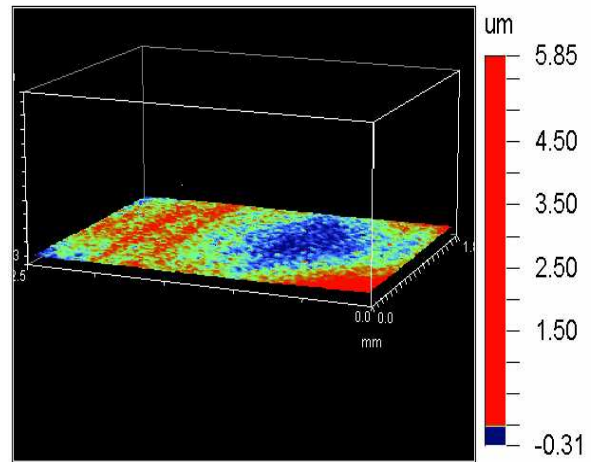


FIG. 8: Image of OTS treated 350 nm-thick SiO_2 surface.

Optical microscopy images of the semiconductor crystals deposited in the channel between source and drain on 350 nm-thick SiO_2 and on OTS modified surface of 350 nm-thick SiO_2 are shown in Figure 9 and 10, respectively. They were obtained with an OLYMPUS PMG3 microscope ($50\times - 1,000\times$ magnification) and they suggest that by modifying the surface using OTS we are able to get larger and better-ordered crystals compared to those obtained with SiO_2 surfaces without modification.

Conclusions

We have thus far been able to study modified SiO_2 surfaces for organic thin film transistors. FTIR results were taken during each step of the modification process, but there was no obvious evidence showing that $-OH$, HMDS or OTS had already bonded onto the SiO_2 surface. However, contact angle measurements suggest that OTS and HMDS are bonded onto the surface. Also, so far, we have not been able to get the transistors we have made to work. Thicker layers of SiO_2 would be used

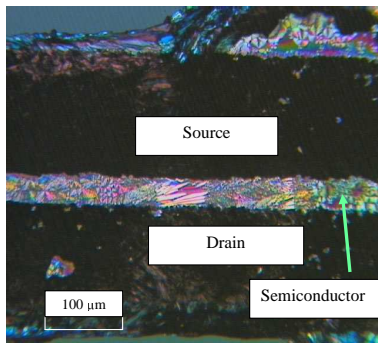


FIG. 9: Crystal structure of semiconductor deposited in the channel between source and drain on 350 nm-thick SiO_2 .

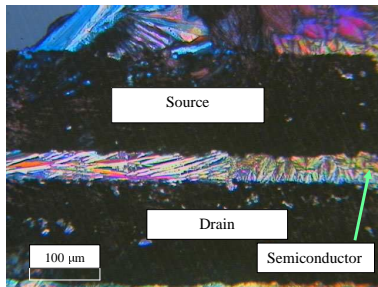


FIG. 10: Crystal structure of semiconductor deposited in the channel between source and drain on OTS surface modified 350 nm-thick SiO_2 .

and techniques like shadow mask would be used to get the source and drain on the substrates. The gate voltage may also be lowered. All these changes will be investigated in order to get the devices to work.

The crystal structure of the semiconductor was also shown to improve upon deposition on OTS treated surfaces as opposed to SiO_2 surfaces. We would still continue to work on getting good crystal structure for the semiconductor layer as well as uniform surfaces of the deposited dielectric films. Future work would include the use plastic substrates and aluminum gates.

Acknowledgements

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¹ C. D. Dimitrakopoulos and D. J. Masearo, IBM Journal Of Research And Development **45**, 11 (2001).

² J. M. Shaw and P. F. Seidler, IBM Journal Of Research And Development **45**, 3 (2001).